

(19)



Generated Document.

(11) Publication number: **05062911 A****PATENT ABSTRACTS OF JAPAN**(21) Application number: **03223234**(22) Application date: **04.09.91**

(51) Intl. Cl.: H01L 21/205 H01S 3/18

(30) Priority:

(43) Date of application 12.03.93  
publication:

(84) Designated contracting states:

(71) Applicant: FUJITSU LTD

(72) Inventor: NAKAI KENYA

(74) Representative:

**(54) MANUFACTURE OF SEMICONDUCTOR SUPERLATTICE**

(57) Abstract:

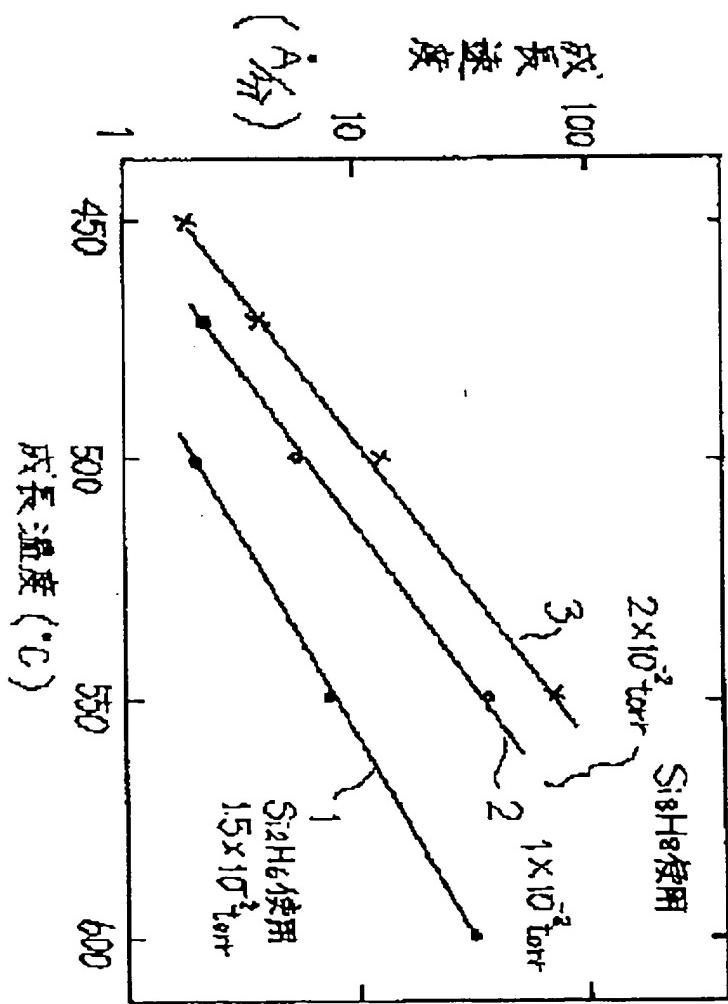
**PURPOSE:** To form a Ge layer and an Si layer or a Ge-Si layer and an Si layer on an Si substrate, and also to put a hetero-epitaxial growth method, in which excellent crystal quality and high growth speed can be obtained, into practical use.

**CONSTITUTION:** The title semiconductor superlattice

manufacturing method is the method with which a Ge layer and an Si layer or Ge-Si layer and an Si layer are epitaxially grown on an Si substrate by conducting a depressed CVD method under the atmosphere

containing oxidizing impurity gas of 1000ppb or lower using GeH<sub>4</sub> and trisilane (Si<sub>3</sub>H<sub>8</sub>) as raw gas and also using H<sub>2</sub> or inert gas as carrier gas.

COPYRIGHT: (C)1993,JPO&Japio



05062911 A

ر ا م د ن د

<http://www.delphion.com/cgi-bin/viewpat.cmd/JP05062911A2>

5/10/01